UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,266	03/31/2004	Douglas Holberg	CYGL-26,655	9833

25883 7590 10/20/2006

HOWISON & ARNOTT, L.L.P
P.O. BOX 741715
DALLAS, TX 75374-1715

EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,266	HOLBERG ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The informal drawings are not of sufficient quality to permit examination. Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to this Office action. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

Applicant is given a TWO MONTH time period to submit new drawings in compliance with 37 CFR 1.81. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a). Failure to timely submit replacement drawing sheets will result in ABANDONMENT of the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and or clarification is required.

Regarding claim 1, the recitation "a first sampling rate" on line 5 is indefinite because it is not clear what it is meant by. This rate could be the frequency of sampling and it could be the time period of time during it sampling happens. The recitations " a first time" on line 6 and "a second time" on line 8 are indefinite because it is not clear what they are meant by. The recitation "dumping charge from the input sampling capacitor to the non-inverting input of the amplifier at a second time and at the first sampling rate " is indefinite because it is confusing. Assume that the rate is the high time period when the charge is dumped to the non-inverting input, figure 2 of the present application shows that the charge is dumped at a "rate" (high level of clock Φ2) is different from the "a first sampling rate" " (high level of clock Φ1). Note that figure 1 of the present application shows that the reference voltage and the input voltage are sampled with different clock rates. The recitation "...at substantially the first sampling rate" on line 9-10 is indefinite because it is misdescriptive. Figure 1 of the present application shows that the input voltage and the reference voltage are sampled with different clock signals i.e., different sampling rate. The recitation " first sampling rate" on line 10 is indefinite because it is not clear as to this "first sampling rate" is the same or different than the "first sampling rate" in line 5. The recitation " a second sampling rate" on line 12 is indefinite because it is not clear what it is meant by. The recitation "controlling the amount of time that charge is dumped from the feedback sampling capacitor to be substantially equal to the amount of time that charge is being dumped from the input sampling capacitor" is indefinite because it is misdescriptive Figure 1 shows that the "charge is dumped from the feedback sampling capacitor" with clock Φ2. ΦA and the "charge is dumped from the input sampling capacitor" with clock Φ2. These clocks are not similar. The Applicant is requested to explain clearly what are the "a first sampling rate", " a first time", "a second time", "a second sampling rate". The same rationale is true for the recitation " the first sampling rate" in claim 2.

Claims 3-8 are indefinite because of the technical deficiencies of claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin (USP. 6,107,871).

Regarding claim 1, figurer 6, 7 and 8 of Shin shows a method for driving the input of an integrator in a delta-sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a reference voltage and an integration capacitor connected between the non-inverting input and the output, comprising the steps of:

sampling an input voltage (Vinp) at a "first sampling rate" with clock (Ø1) onto an input sampling capacitor (C/4) "at a first time";

dumping charge from the input sampling capacitor (C/4) to the non-inverting input of the amplifier at "a second time" with clock (Ø2) at the "second sampling rate";

sampling a reference voltage (Vinp) onto a input sampling capacitor (C/4) at substantially the "first clock rate" (Ø1);

dumping charge stored on the feedback sampling capacitor (C/4) to the non-inverting input of the amplifier at a "second sampling rate" (Ø2) different than the first rate (Ø1); and

controlling the amount of time by varying the duty cycle of signal (Ø2) that charge is dumped from the feedback sampling capacitor (C/4) to be substantially equal to the amount of time that charge is being dumped from the input sampling capacitor (note that the dumping of the charges onto the negative feedback of the amplifier is performed with the same clock signal (Ø2);

wherein varying the "second sampling rate" (Ø2) relative to the "first sampling rate" change the gain of the delta-sigma converter.

Regarding claims 2 and 3, the steps of sampling an input voltage at the "first sampling rate" (Ø1) onto an input sampling capacitor (C/4) and dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprise:

generating a first sampling (Ø1) with a first stream of periodic pulses at the "first sampling rate";

generating a second sampling (Ø2) with a second stream of periodic pulses and shifted in phase from the first sampling and synchronous therewith;

sampling the input voltage (Vinp) onto the input sampling capacitor (C/4) during the time that the first stream of pulses (Ø1) are high; and

dumping charge from the input sampling capacitor (C/4) to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high. Pulses (Ø1) and (Ø2) are non-overlapping

Regarding claim 4, the step of sampling the input voltage on the input sampling capacitor comprises the steps of connecting one plate of the input sampling capacitor (C/4) to the input voltage (Vinp) and the other plate of the input sampling capacitor to ground during the time that the first stream of pulses (Ø1) are high; and

the step of dumping charge from the input sampling capacitor to the non-inverting input of the amplifier comprises the steps of connecting the one plate of the input sampling capacitor (C/4) to ground and the other plate of the input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high.

Regarding claim 5, the steps of sampling the reference voltage onto the feedback sampling capacitor and dumping charge stored on the feedback sampling capacitor to the non- inverting input of the amplifier comprises the steps of:

sampling the reference voltage (Vinn) onto the feedback sampling capacitor (C/4) during the time that the first stream of pulses (Ø1) are high; and

dumping charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high and at a different rate than the step of sampling the reference voltage onto the feedback sampling capacitor.

Regarding claim 6, the step of sampling the reference voltage on the feedback sampling capacitor comprises the steps of connecting one plate of the feedback sampling

capacitor (C/4) to the reference voltage (Vinn) and the other plate of the feedback sampling capacitor to ground during the time that the first stream of pulses (Ø1) are high; and the step of dumping charge from the feedback sampling capacitor (C/4) to the non-inverting input of the amplifier comprises the steps of connecting the one plate of the feedback sampling capacitor to ground and the other plate of the feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high and at a different rate than the step of sampling the reference voltage onto a feedback sampling capacitor. Note that signals (Ø1) and (Ø2) have different duty cycles.

Regarding claim 7, the step of dumping charge stored on the feedback sampling capacitor (C/4) to the non-inverting input of the amplifier occurs during the time that select ones of the pulses in the second stream of pulses are high, and the number of the pulses in the second stream of pulses during which the step of dumping charge stored on the feedback sampling capacitor to the non- inverting input of the amplifier is less than all of the pulses in the second stream of pulses.

Regarding claim 8, the step of generating a control signal in a control circuit, not shown, that generates and regulating signals (Ø1) and (Ø2), that selects the ones of the pulses in the second stream of pulses during which charge stored on the feedback sampling capacitor (C/4) is dumped to the non-inverting input of the amplifier with clock (Ø2),.

Regarding claim 9, figure 6 of Shin shows a gain control circuitry for driving the input of an integrator in a delta-sigma converter having an amplifier with a non-inverting input, an output and a positive input connected to a reference voltage and an integration capacitor connected between the non-inverting input and the output comprising:

an input sampling circuit (SW1, SW4) for sampling an input voltage at a "first clock rate" (duty cycle) (Ø1) onto an input sampling capacitor (C/4);

a first dump circuit (SW2, SW3) for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier at a second duty cycle of clock (Ø2);

a feedback sampling circuit (SW13, SW16) for sampling a reference voltage (Vinn) onto a feedback sampling capacitor at substantially the "first sampling" (Ø1);

a second dump circuit (SW14, SW15) for dumping charge stored on said feedback sampling capacitor (C/4) to the non-inverting input of the amplifier at a "second sampling rate" (Ø2) different than the first sampling rate;

a gain controller, not shown, for controlling the amount of time (the duty cycle of Ø2) that charge is dumped from said feedback sampling capacitor (C/4) to be substantially equal to the amount of time (Ø2) that charge is being dumped from said input sampling capacitor;

wherein varying the second sampling rate relative to the first sampling rate changes the gain of delta-sigma converter.

Regarding claim 10, the first dump circuit comprises:

a first sampling clock for generating a first stream of periodic pulses (Ø1) at the "first sampling rate";

a second clock for generating a second stream of periodic pulses (Ø2);

first switching circuitry (SW1, SW4) for sampling the input voltage onto the non-inverting input of the amplifier during the time that the first stream of pulses (Ø1) are high; and

second switching circuitry (SW2, SW3) for dumping charge from said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high.

Regarding claim 11, the first stream of periodic pulses and said second stream of periodic pulses are non overlapping (Fig. 8).

Regarding claim 12, the first switching circuitry includes

a first switch (SW1) for connecting one plate of said input sampling capacitor to the input voltage, and

a second switch SW4) for connecting the other plate of said input sampling capacitor to ground during the time that the first stream of pulses are high; and

said second switching circuitry includes:

a third switch (SW3) for connecting the one plate of said input sampling capacitor to ground, and

a fourth switch (SW2) for connecting the other plate of said input sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) is high.

Regarding claim 13, the second sampling circuit and said second dump circuit comprise:

third switching circuitry (SW13, WS16) for sampling said reference voltage (Vinn) onto the non-inverting input of the amplifier during the time that the first stream of pulses (Ø1) are high; and

second switching circuitry (SW14, SW15) for dumping charge from said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high and at a different sampling rate than the sampling rate at which the reference voltage is sampled onto said feedback sampling capacitor.

Regarding claim 14, the third switching circuitry includes:

a fifth switch (SW13) for connecting one plate of said feedback sampling capacitor to the reference voltage (VINN), and

a sixth switch (SW16) for connecting the other plate of said feedback sampling capacitor to ground during the time that the first stream of pulses are high; and said fourth switching circuitry includes:

a seventh switch (SW15) for connecting the one plate of said feedback sampling capacitor to ground, and

an eighth switch (SW14) for connecting the other plate of said feedback sampling capacitor to the non-inverting input of the amplifier during the time that the second stream of pulses (Ø2) are high and at a different sampling rate than the sampling ate at which the reference voltage is sampled onto said feedback sampling capacitor.

Regarding claim 15, the dumping of charge stored on said feedback sampling capacitor to the non-inverting input of the amplifier occurs during the time that select ones of the pulses in the second stream of pulses (Ø2), and the number of the pulses in the second stream of pulses during which dumping of charge stored on the feedback sampling capacitor to the non-inverting input of the amplifier is less than all of the pulses in the second stream of pulses (Fig. 8).

Regarding claim 16, the control signal (not shown) that selects the ones of the pulses in the second stream of pulses (Ø2) during which charge stored on the feedback sampling capacitor is dumped to the non-inverting input of the amplifier.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen
10-17-06

TUAN T. LAM
PRIMARY EXAMINER